Abstract of the Disclosure:

A synchronous integrated memory for holding data includes an output circuit that can be activated through an activation connection that, in the activated state, starts an output process for data to be read out in synchronism with a first internal clock, and outputs the data with a specific phase shift with respect to the first internal clock in synchronism with an external clock at a data connection. A counting unit starts a counting process for recording the number of successively following first levels of the first internal clock as soon as a second internal clock, which is synchronized to the external clock, for the first time assumes a first level while an output control signal is at the first level. It activates the output circuit as soon as the number of successively following first levels of the first internal clock has reached a predetermined value.

GLM